

Panasonic Liquid Crystal Display Co.,Ltd.

For Messrs. Panasonic Corporation Group

TECHNICAL DATA

VVX19H101G00

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RECORD OF REVISION

Date	The upper section : Previous revision The lower section : New revision		Summary
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DESCRIPTION

The following specifications are applied to the following IPS-Pro-TFT LCD module.

Note : The timing controller function is not built in this module.

MODEL No. : VVX19H101G00

GENERAL SPECIFICATIONS

Effective display area	: (H) 409.8 × (V) 230.4	(mm)
Number of pixels	: (H) 1,366 × (V) 768	(pixels)
Pixel pitch	: (H) 0.300 × (V) 0.300	(mm)
Color pixel arrangement	: R+G+B vertical stripe	
Display mode	: Transmissive mode Normally black mode	
Top polarizer type	: Semi-Glare	
Viewing angle range	: Wide version (Horizontal & vertical : 178° at $\theta = 0^\circ, 90^\circ, 180^\circ, 270^\circ$, $CR \geq 10$)	
Input signal	: miniLVDS (LVDS : Low voltage differential signaling)	
Backlight	: LED	
External dimensions	: (H)430.4 × (V)254.6 × (t)12.4 typ(mm) The thickness to the bottom plate is 7.7mm.	
Weight	: 1,070	(g)

1. ABSOLUTE MAXIMUM RATINGS

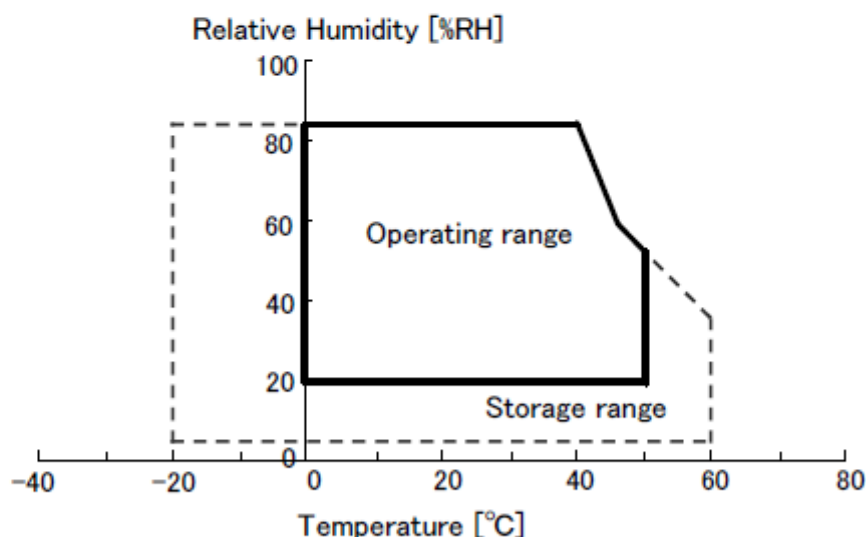
1.1 ENVIRONMENT ABSOLUTE MAXIMUM RATINGS

ITEM	Value		Unit	Note
	MIN.	MAX.		
Storage Temperature	-20	60	°C	(1),(2),(5)
Operating Temperature	0	50	°C	(1),(2),(5)
Humidity	(2)		%RH	(1)
Vibration	—	14.7 (1.5G)	m/s ²	(3)
Shock	—	294(30G)	m/s ²	(4)

Note (1) Temperature and Humidity should be applied to the glass surface of a IPS-Pro TFT LCD module, not to the system installed with a module.

Note (2) $T_a \leq 40^{\circ}\text{C}$ Relative humidity should be less than 85 %RH max. Dew is prohibited.

$T_a > 40^{\circ}\text{C}$ Relative humidity should be lower than the moisture of the 85 %RH at 40 °C.



Note (3) Frequency of the vibration is between 15 Hz and 100 Hz. (Remove the resonance point) 1 hour.

Note (4) Pulse width of the shock is 10 ms.

Note (5) The temperature of LCD front surface would be 65 °C in operating, it may affect the optical characteristics however it does not damage the function of the module.

1. 2 Electrical Absolute Maximum Ratings

(1) TFT-LCD module

V_{SS} = 0 V

ITEM	SYMBOL	Min.	Max.	UNIT	NOTE
Source Driver Analog Power Supply	AVDD	0	17.0	V	
Driver Logic Power Supply	VDD	0	4.0	V	
Gate Driver Power Supply	VON	0	37	V	
	VON-VOFF	0	44	V	
Gate Driver Ground	VOFF	-20	0.3	V	
Gamma Corrected Power Supply	VREF1~6	0.4AVDD	AVDD+0.3	V	
Gamma Corrected Power Supply	VREF8~12	-0.3	0.6AVDD	V	
Common Plate Power Supply	VCOM	VCOMaj - 2.0	VCOMaj + 2.0	V	5)
Input Voltage for logic	V ₁	-0.3	VDD + 0.3	V	1)
	V ₂	-0.3	VDD + 1.2	V	6)
	V ₃	-0.3	7	V	7)
Electrostatic Durability	V _{ESD0}	±100		V	2),3)
	V _{ESD1}	±20		kV	2),4)

Note 1) It is applied to pixel data signal, clock signal and other control signals.

2) Discharge Coefficient : 250 pF - 100 Ω, Environmental : 25 °C - 70%RH

3) It is applied to I/F connector pins.

4) It is applied to the surface of a metallic bezel and a LCD panel.

5) VCOMaj means adjusted VCOM voltage.

6) It is applied to SDA, SCL signal.

7) It is applied to WP signal.

(2) Backlight unit

ITEM	SYMBOL	Min.	Max.	UNIT	NOTE
Power Supply Voltage	V _{BL}	0	34	V	
ON/OFF Control Voltage	V _{ON} /V _{OFF}	0	VBL	V	
PWM Signal Voltage	V _{PWM}	0	20	V	

2. INITIAL OPTICAL CHARACTERISTICS

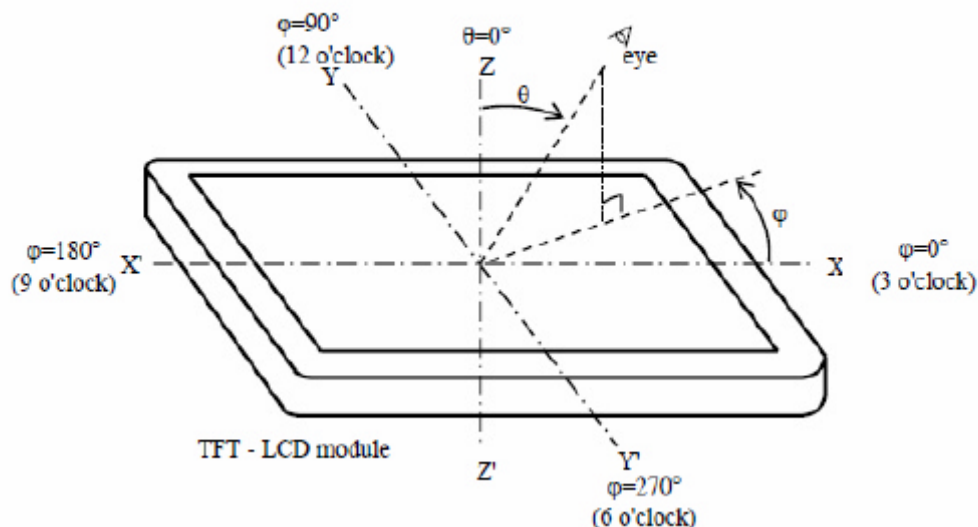
2.1 TEST CONDITIONS

- (1) Environmental Temperature : $25 \pm 5^\circ\text{C}$.
- (2) Dark Room : under 10 LX, no wind.
- (3) Lighting after 30 min.
- (4) Measuring equipment : SR-3A, or equivalent

2.2 OPTICAL SPECIFICATIONS

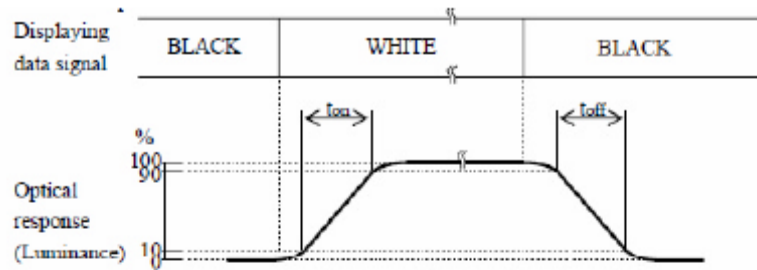
Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	$\theta = 0^{\circ}$ Viewing Normal Angle (1)	600	1000	—	—	(2)
Response Time		t_{ON}		—	8	20	ms	(3)
		t_{OFF}		—	6	20	ms	
Center Luminance of White		L_C		200	250	—	cd/m^2	
White Variation		σW		—	—	30	%	(4)
Color Chromaticity	Red	R_x		$\text{Typ} - 0.03$	$\text{Typ} + 0.03$	—		
		R_y						
	Green	G_x						
		G_y						
	Blue	B_x						
		B_y						
	White	W_x						
		W_y						
Variation of Color position (CIE)	Red	R_x	$\theta = 50^{\circ}$ $\phi = 0^{\circ}, 90^{\circ}, 180^{\circ}, 270^{\circ}$ (1)	—	—	0.04	—	(5)
		R_y		—	—	0.04		
	Green	G_x		—	—	0.04		
		G_y		—	—	0.04		
	Blue	B_x		—	—	0.04		
		B_y		—	—	0.04		
	White	W_x		—	—	0.04		
		W_y		—	—	0.04		
	Contrast Ratio at 89°			CR89	(6)	10		
Image sticking		—	Mosaic Pattern	Invisible			—	(7)

Note (1) Definition of viewing angle



Note (2) Definition of contrast ratio (CR).
 $CR = (\text{Luminance at displaying WHITE}) / (\text{Luminance at displaying BLACK})$

Note (3) Definition of response time

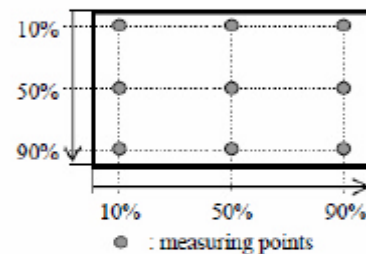


Note (4) Definition of brightness uniformity
 Display pattern is white (1023 level) .
 The brightness uniformity is defined as the following equation.
 Brightness at each point is measured, and average, maximum and minimum brightness is calculated.

$$B_{uni} = \frac{|B_{max} \text{ or } B_{min} - B_{ave}|}{B_{ave}} \times 100$$

where, B_{max} = Maximum brightness
 B_{min} = Minimum brightness
 B_{ave} = Average brightness

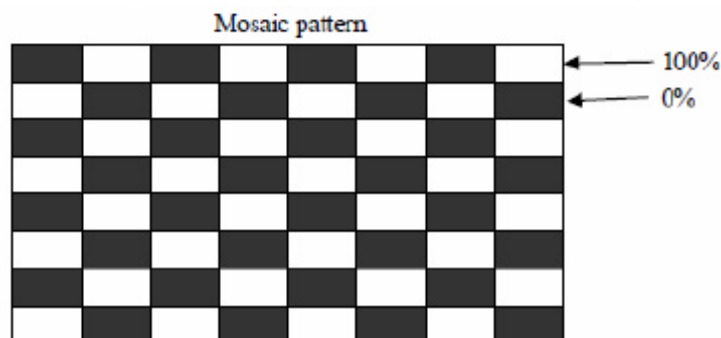
$$B_{ave} = \frac{\sum_{k=1}^9 (B(k))}{9}$$



Note (5) Variation of color position on CIE
 Variation of color position on CIE is defined as difference between colors at $\theta = 0^\circ$ and at $\theta = 50^\circ$ & $\phi = 0^\circ, 90^\circ, 180^\circ, 270^\circ$.

Note (6) Contrast ratio at 89°
 Evaluation conditions are on horizontal & vertical axis.

Note (7) Image sticking
 Condition : Operating mosaic pattern for 2 hours and gray scale (22 %) for 1 hour.



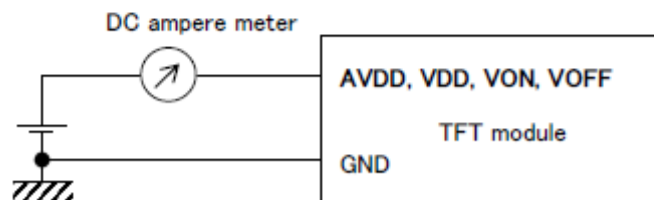
3. ELECTRICAL CHARACTERISTICS

3.1 TFT-LCD module

Ta = 25 °C, Vss = 0 V

ITEM	SYMBOL	Min.	Typ.	Max.	UNIT	NOTE
Source Driver Analog Power Supply Voltage	AVDD	12.7	13.0	13.3	V	
Ripple voltage of AVDD	Vrip_avdd	—	—	380	mV	5), 6)
Driver Logic Power Supply Voltage	VDD	2.4	2.5	2.6	V	
Ripple voltage of VDD	Vrip_vdd	—	—	150	mV	5), 6)
Gate Driver Power Supply Voltage	VON	29.0	30.5	32.5	V	
Ripple voltage of VON	Vrip_von	—	—	500	mV	5), 6)
Gate Driver Ground Voltage	VOFF	-6.35	-5.8	-5.25	V	
Ripple voltage of VOFF	Vrip_voff	—	—	200	mV	5), 6)
Input High Voltage for logic	VIH1	0.8VDD	—	VDD	V	2)
Input Low Voltage for logic	VIL1	0	—	0.2VDD	V	2)
Input High Voltage for EEPROM	VIH2	0.8VDD	—	VDD+1.2	V	3)
	VIH3	0.8VDD	—	5.25	V	7)
Input Low Voltage for EEPROM	VIL2	0	—	0.2VDD	V	3)
Output Low Voltage from EEPROM	VOL	—	—	0.4	V	4)
Common Plate Voltage	VCOM	—	4.116	—	V	
Ripple voltage of VCOM	Vrip_vcom	—	—	200	mV	5), 6)
Source Driver Analog Power Supply Current	IADD	—	150	360	mA	1)
Driver Logic Power Supply Current	IDD	—	30	80	mA	1)
Gate Driver Power Supply Current	ION	—	3.0	5.0	mA	1)
Gate Driver Ground Current	IOFF	-5.0	-3.0	—	mA	1)
Gamma Corrected Power Supply Voltage 1	VREF1	—	12.525	—	V	
Gamma Corrected Power Supply Voltage 2	VREF2	—	10.924	—	V	
Gamma Corrected Power Supply Voltage 3	VREF3	—	9.565	—	V	
Gamma Corrected Power Supply Voltage 4	VREF4	—	8.930	—	V	
Gamma Corrected Power Supply Voltage 5	VREF5	—	8.409	—	V	
Gamma Corrected Power Supply Voltage 6	VREF6	—	6.580	—	V	
Gamma Corrected Power Supply Voltage 8	VREF8	—	4.662	—	V	
Gamma Corrected Power Supply Voltage 9	VREF9	—	4.116	—	V	
Gamma Corrected Power Supply Voltage 10	VREF10	—	3.443	—	V	
Gamma Corrected Power Supply Voltage 11	VREF11	—	2.033	—	V	
Gamma Corrected Power Supply Voltage 12	VREF12	—	0.343	—	V	
Ripple voltage of VREF	Vrip_VREF	—	—	200	mV	5), 6)

Note 1) fV=60.0Hz, fCLK=156MHz, each power supply voltage is typical condition and display pattern is white raster.



- 2) It is applied to LP, POLR, POLL, CPV, DATA1 and DATA2 signal.
- 3) It is applied to SDA, SCL signal.
- 4) It is applied to SDA signal.
- 5) The above specification is defined at connector CN1.
- 6) Display pattern is white raster.
- 7) It is applied to WP signal.

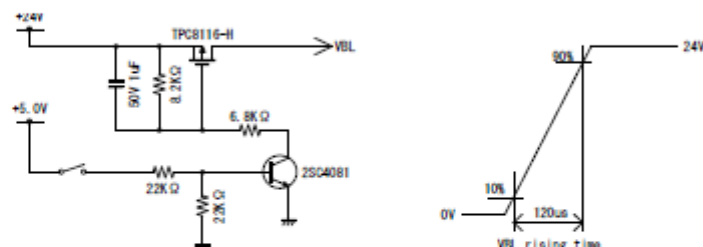
3.2 BACKLIGHT UNIT

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Input Voltage	VBL	21.6	24	26.4	V	
Input Current	IBL	—	0.63	—	A	PWM ON Duty Ratio: 100%.
Peak Current	IBL_PEAK	—	—	1.5	A	(1)
Rush Current 1	IBL_RUSH	—	3.5	—	A	(2) VBL Input Rush
Rush Current 2	IBL_RUSH	—	5.5	—	A	(4) Von HI Keeping PWM 0%→100% Turn On
Standby Current	I _{ST}	—	15	25	uA	ON/OFF Control Voltage : 0V
VBL Rising Time	tr_VBL	120	—	—	usec	
ON/OFF Control Voltage	ON	V _{ON}	2.0	—	VBL	V
	OFF	V _{OFF}	0.0	—	0.8	V
PWM Signal	Hi	V _{PWM}	2.2	—	5.5	V
	Low		0.0	—	0.8	V
Diming Frequency	F _{PWM}	90	180	200	Hz	
ON Duty Ratio	D _{PWM}	0	—	100	%	(3)(4)
Power Consumption	P _F	—	15.2	16.2	W	
LED Life Time	—	30,000	—	—	hours	(5)

Note(1) PWM ON Duty Ratio adjusted less than 100%, Diming Frequency : 180Hz.

Note(2) Measurement conditions:

The duaring of rising time of power input 120us.



Note(3) If you turn on PWM, please do from 0% to duty ratio more than 1%.

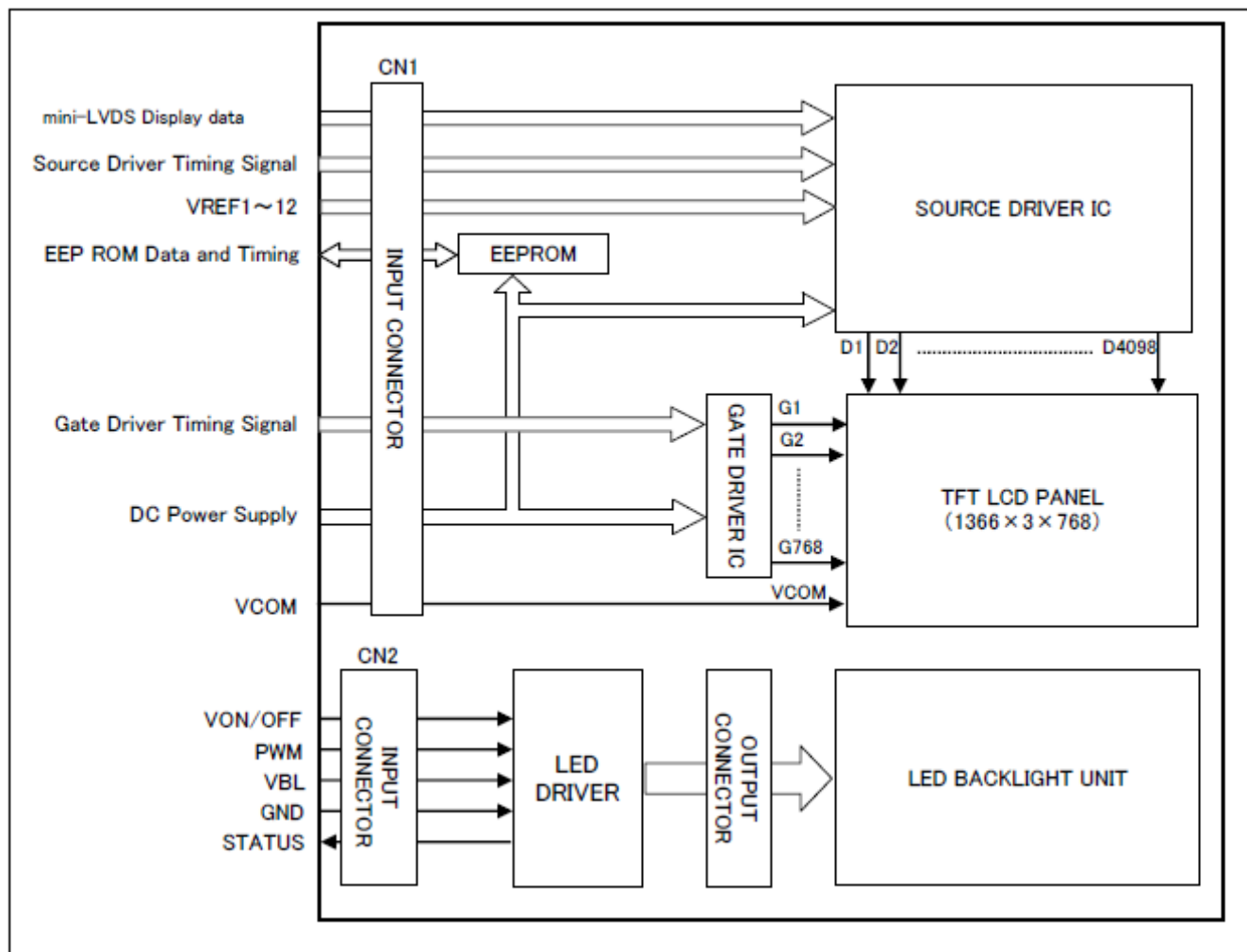
(Please do not do from 0 to duty ratio 0.1~0.9%. Because, there is a possibility of shut down).

Note(4) When on duty ratio becomes 0% ($\geq 80\text{msec}$), It is recommended to restart the on/off control simultaneously the PWM control

The IBL inrush current increases because a soft-start doesn't work.

Note(5) Life time of LED is defined. The life is determined as the time at which brightness of the LED is 50 % compared to that of initial value at that typical LED current on condition of continuous operating at $25 \pm 2^\circ\text{C}$.

4. BLOCK DIAGRAM



5. INTERFACE PIN ASSIGNMENT

5.1 TFT-LCD module

CN1:MOLEX 503366-6011

PIN No.	SYMBOL	DESCRIPTION	NOTE
1	GND	Ground(0V)	3)
2	SCL	I2C-bus Serial Clock	
3	SDA	I2C-bus Serial Data	7)
4	WP	EEPROM Write Protect	6)
5	VREF12	Gamma Corrected Power Supply	
6	VREF11		
7	VREF10		
8	VREF9		
9	VREF8		
10	VCOM	Common Plate Power Supply	
11	VCOM	Power Supply	
12	AVDD	Source Driver Analog Power Supply	1)
13	AVDD		
14	AVDD		
15	AVDD		
16	GND	Ground(0V)	3)
17	VDD	EEPROM Power Supply	2)
18	VDD	Driver	2)
19	VDD	Logic Power Supply	
20	LP	Latch Clock Input	
21	POLR	Polarity Control Input(Left Side)	
22	GND	Ground(0V)	3)
23	CLKL-	mini-LVDS Left Side	5)
24	CLKL+	Pixel Clock	
25	GND	Ground(0V)	3)
26	LV2L-	mini-LVDS Left Side	5)
27	LV2L+	Pixel Data	
28	GND	Ground(0V)	3)
29	LV1L-	mini-LVDS Left Side	5)
30	LV1L+	Pixel Data	

PIN No.	SYMBOL	DESCRIPTION	NOTE
31	GND	Ground(0V)	3)
32	LV0L-	mini-LVDS Left Side	5)
33	LV0L+	Pixel Data	
34	GND	Ground(0V)	3)
35	CLKR-	mini-LVDS Right Side	5)
36	CLKR+	Pixel Clock	
37	GND	Ground(0V)	3)
38	LV2R-	mini-LVDS Right Side	5)
39	LV2R+	Pixel Data	
40	GND	Ground(0V)	3)
41	LV1R-	mini-LVDS Right Side	5)
42	LV1R+	Pixel Data	
43	GND	Ground(0V)	3)
44	LV0R-	mini-LVDS Right Side	5)
45	LV0R+	Pixel Data	
46	GND	Ground(0V)	3)
47	VREF6	Gamma Corrected Power Supply	
48	VREF5		
49	VREF4		
50	VREF3		
51	VREF2		
52	VREF1		
53	NC	No Connection	
54	VON	Gate Driver Power Supply	
55	VOFF	Gate Driver Ground	4)
56	POLL	Polarity Control Input(Right Side)	
57	DATA2	Gate Driver Control Input	
58	DATA1		
59	CPV	Gate Shift Clock Input	
60	GND	Ground(0V)	3)

Notes 1) All AVDD pins shall be connected to +12.586V(Typ.).

2) All VDD pins shall be connected to +2.5V(Typ.).

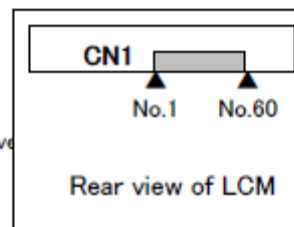
3) All GND pins shall be grounded. Metal bezel is internally connected to GND.

4) All VOFF pins shall be connected to -5.8V(Typ.).

5) LVn+L/R and LVn-L/R (n=0~2) should be wired by side-by-side FFC patterns, respective

6) High level as write enable, Low level or open as write protect

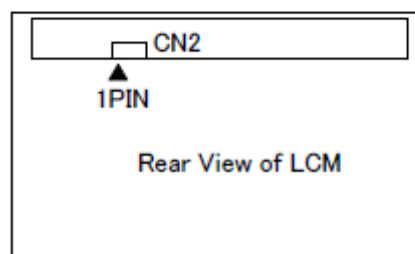
7) EEP-ROM device adress: "1010000"



5.2 Backlight unit

PIN	SYMBOL	Description
1	VBL	Power Supply +24.0V
2	VBL	Power Supply +24.0V
3	VBL	Power Supply +24.0V
4	GND	Backlight Ground
5	GND	Backlight Ground
6	GND	Backlight Ground
7	STATUS	Status Output (Normal: L, Abnormal: OPEN CORRECTOR)
8	VON/VOFF	ON: H, OFF: L
9	EXTVBR-B	External PWM

Connector : SM09B-SRSS-TB (JST)



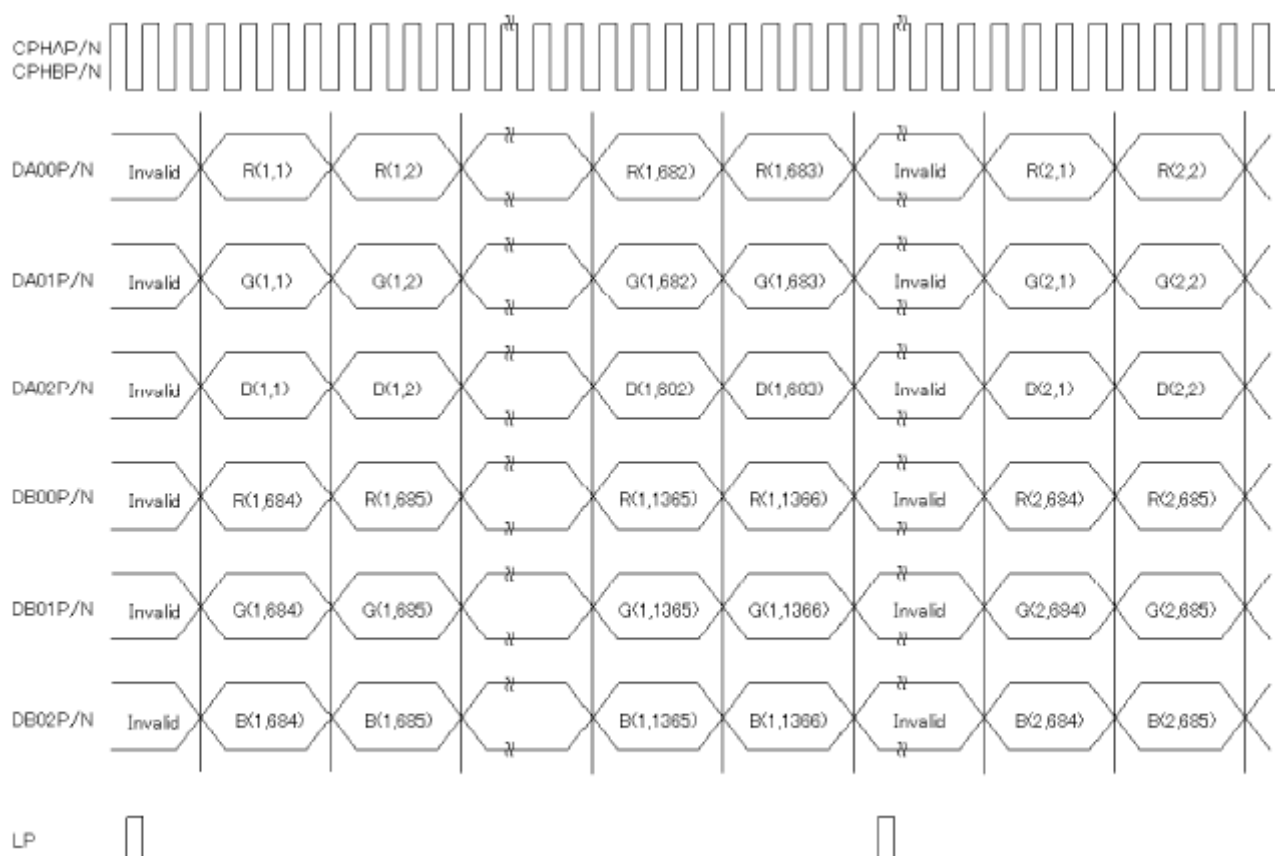
5.3 CORRESPONDENCE BETWEEN INPUT DATA AND DISPLAY IMAGE

Display data of adjacent one pixel is latched during one cycle of DCLK.

R	G	B
(1,1)	(1,1)	(1,1)

Pixel : R0 – R7 : R data
G0 – G7 : G data
B0 – B7 : B data

1, 1	1, 2	...	1,682	1,683	1,684	1,685	...	1,1365	1,1366
2, 1	2, 2	...	2,682	2,683	2,684	2,685	...	2,1365	2,1366
3, 1	3, 2	...	3,682	3,683	3,684	3,685	...	3,1365	3,1366
⋮	⋮		⋮	⋮	⋮	⋮		⋮	⋮
768, 1	768, 2	...	768,682	768,683	768,684	768,685	...	768,1365	768,1366



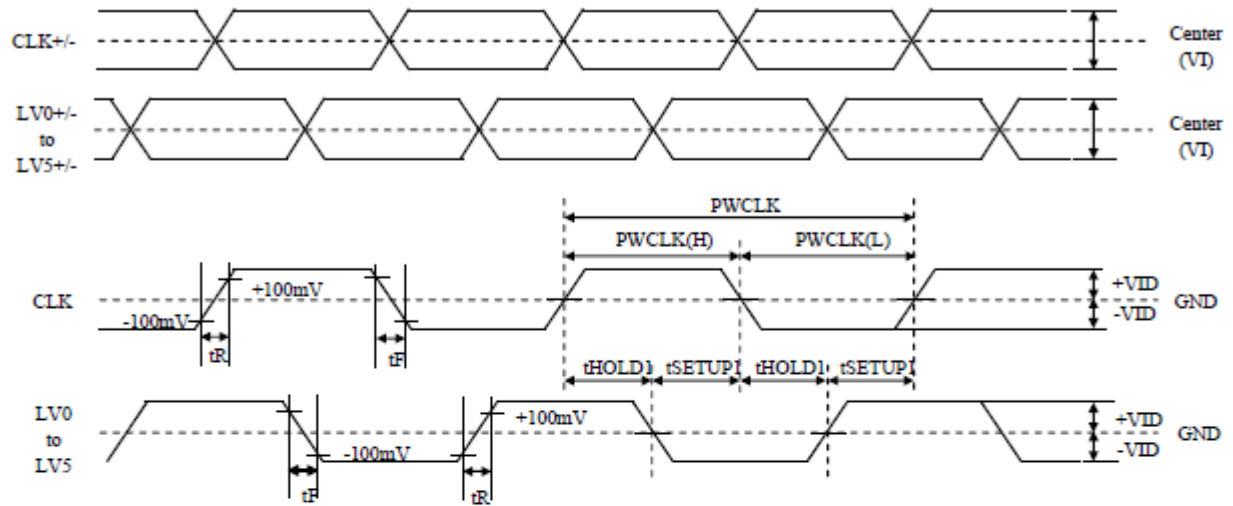
5.4 RELATIONSHIP BETWEEN DISPLAY COLORS AND INPUT SIGNALS

Color		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(253)	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note(1) 0 : Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 mini-LVDS receiver timing



$$LVn = (LVn+) - (LVn-) \quad n=0 \sim 5$$

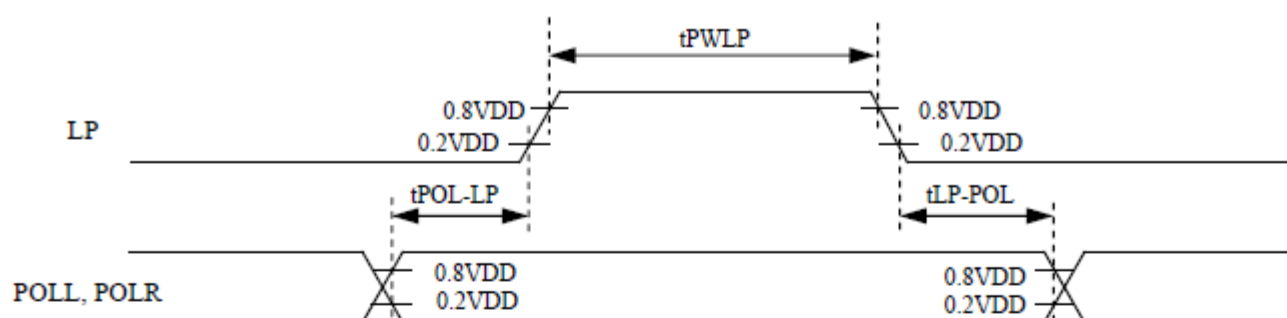
$$CLK = (CLK+) - (CLK-)$$

ITEM	SYMBOL	Min.	Typ.	Max.	UNIT	NOTE
Clock period	PWCLK	5.9	6.4	7.3	ns	
Clock high level width	PWCLK(H)	2.5	3.2	-	ns	
Clock Low level width	PWCLK(L)	2.5	3.2	-	ns	
Data setup time	tSETUP1	1.0	-	-	ns	
Data hold time	tHOLD1	1.0	-	-	ns	
mini-LVDS rise time	tR	-	-	0.8	ns	
mini-LVDS fall time	tF	-	-	0.8	ns	
mini-LVDS differential voltage	VID	100	-	600	mV	
mini-LVDS common mode input voltage range	VI	0.3+VID/2	-	VDD-1.3 -VID/2	V	

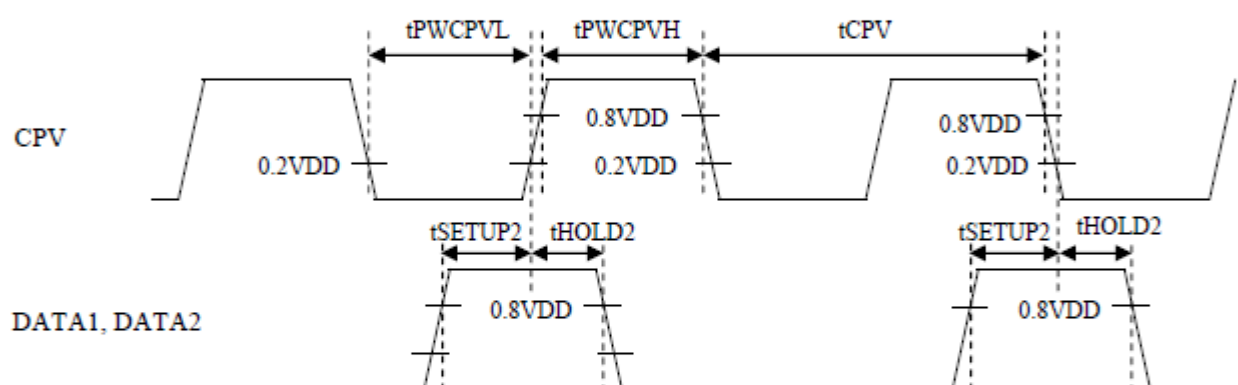
Notes 1) The above specification is defined at each Source Driver IC inputs.

6.2 Control signal timing

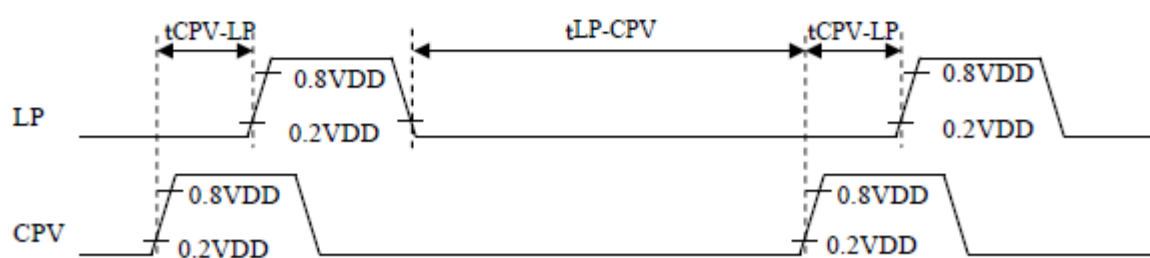
Notes 1) The following specification is defined at connector CN1.



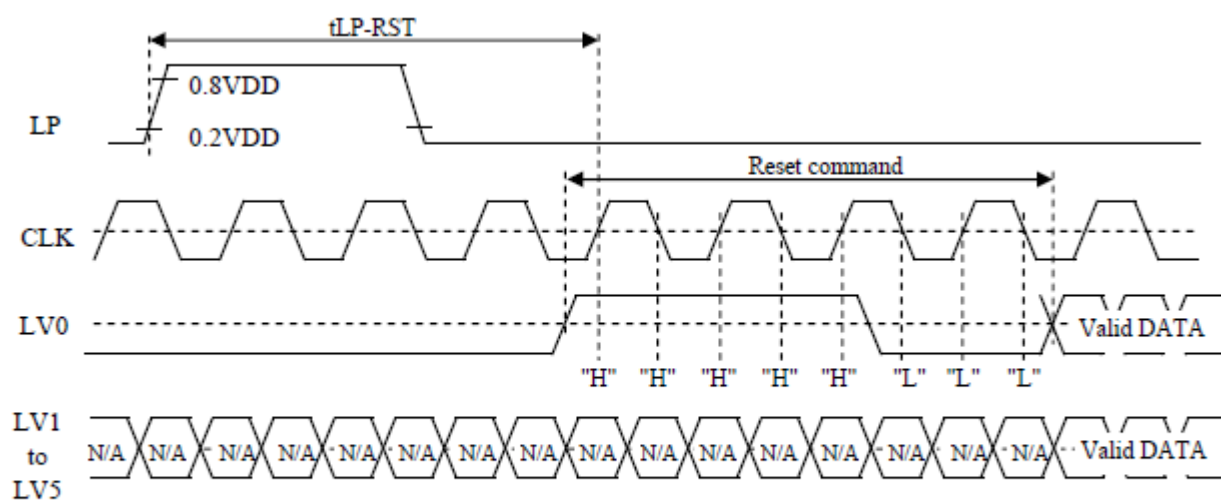
ITEM	SYMBOL	Min.	Typ.	Max.	UNIT	NOTE
Latch clock high level width	t_{PWLP}	1500	1580	—	ns	
POL setup time	t_{POL-LP}	100	—	—	ns	
POL hold time	t_{LP-POL}	100	—	—	ns	



ITEM	SYMBOL	Min.	Typ.	Max.	UNIT	NOTE
Gate shift clock period	t_{CPV}	20	—	—	μs	
Gate shift clock high level width	t_{PWCPVH}	500	—	—	ns	
Gate shift clock low level width	t_{PWCPVL}	500	—	—	ns	
Data setup time	t_{SETUP2}	200	—	—	ns	
Data hold time	t_{HOLD2}	200	—	—	ns	



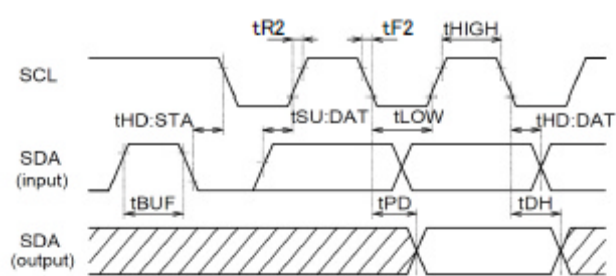
ITEM	SYMBOL	Min.	Typ.	Max.	UNIT	NOTE
Gate delay time	t_{CPV-LP}	5.8	—	—	μs	
TFT charge time	t_{LP-CPV}	11	12	—	μs	



ITEM	SYMBOL	Min.	Typ.	Max.	UNIT	NOTE
Reset input time	tLP-RST	500	—	—	ns	

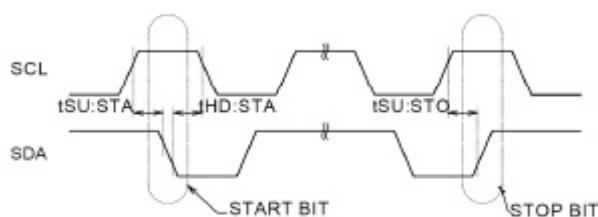
6.3 I2C BUS timing

Notes 1) The following specification is defined at connector CN1.

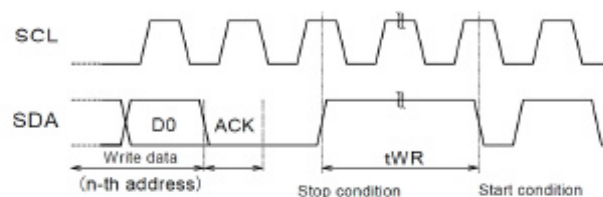


Measurement condition

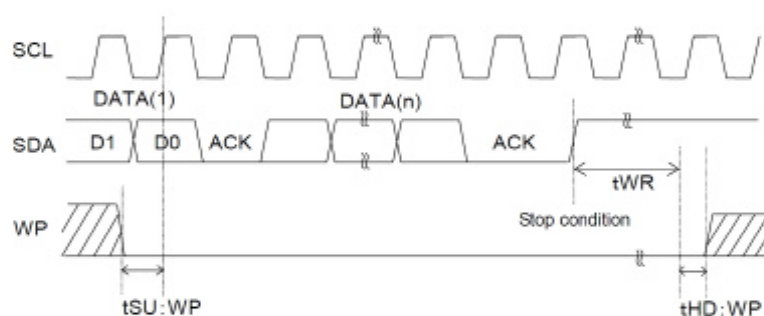
Sync data input/output timing



Start-stop bit timing



Write cycle timing



WP timing at write execution

ITEM	SYMBOL	Min.	Typ.	Max.	UNIT	NOTE
SCL frequency	fSCL	—	—	100	kHz	
Data clock high level width	tHIGH	4.1	—	—	us	
Data clock low level width	tLOW	4.8	—	—	us	
SDA, SCL rise time	tR2	—	—	0.9	us	
SDA, SCL fall time	tF2	—	—	0.2	us	
Start condition hold time	tHD:STA	4.1	—	—	us	
Start condition setup time	tSU:STA	4.8	—	—	us	
Input data hold time	tHD:DAT	50	—	—	ns	
Input data setup time	tSU:DAT	250	—	—	ns	
Output data delay time	tPD	80	—	4000	ns	
Output data hold time	tDH	50	—	—	ns	
Stop condition setup time	tSU:STO	4.1	—	—	us	
Bus release time	tBUF	4.8	—	—	us	
Internal write cycle time	tWR	—	—	11	ms	
WP hold time	tHD:WP	0.1	—	—	ns	
WP setup time	tSU:WP	2.0	—	—	us	

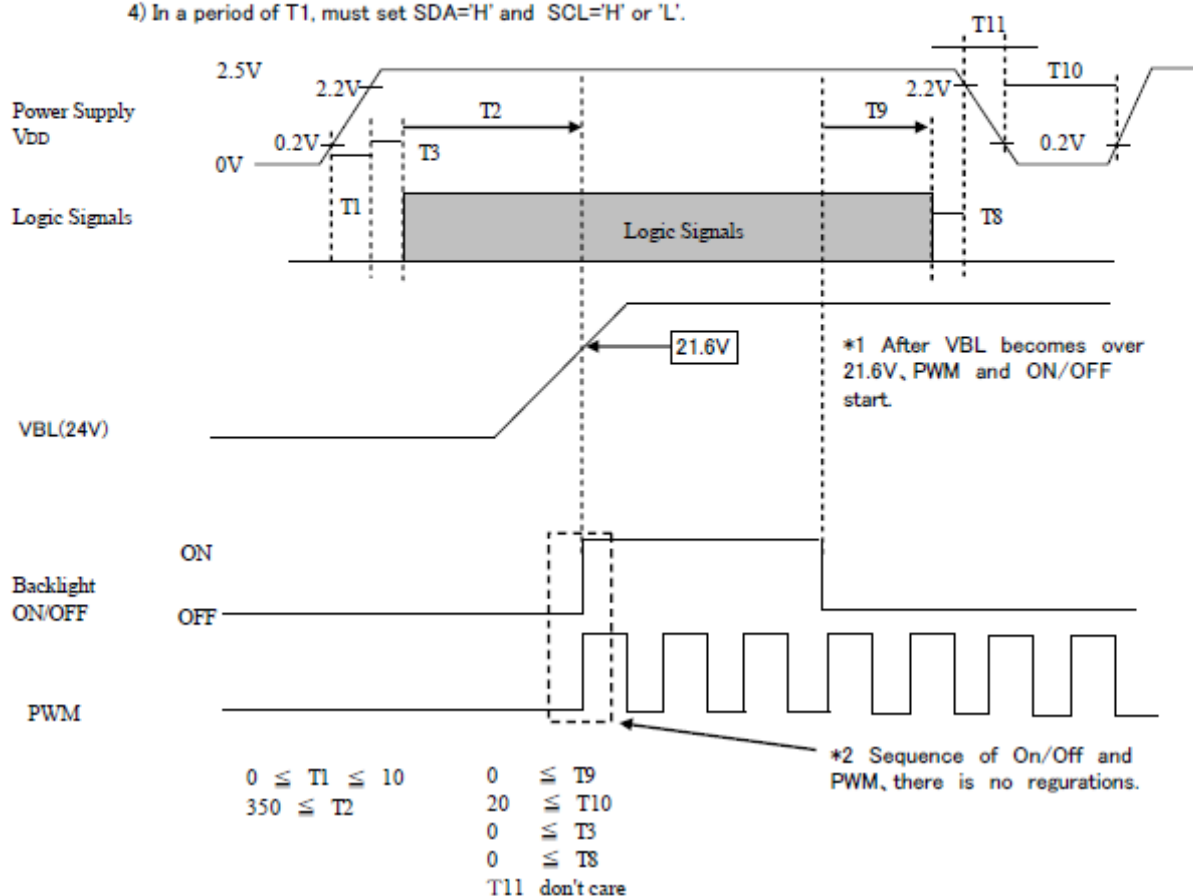
6.4 Timing between interface signals power supply

Notes 1) The following specification is defined at connector CN1.

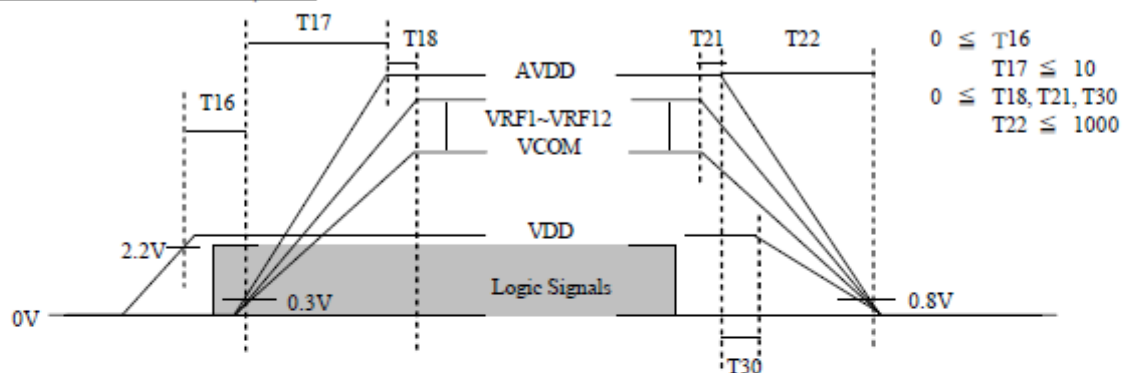
2) In the T16 and T17, the float equal to or less than 1.5V of AVDD is no object.

3) In the T24 and T25, the float equal to or less than 1.5V of VON is no object.

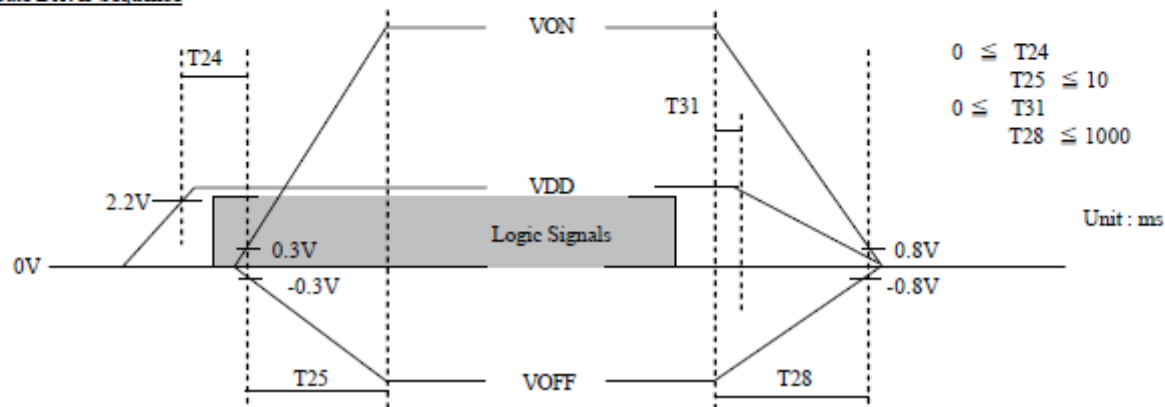
4) In a period of T1, must set SDA='H' and SCL='H' or 'L'.



Source Driver & VCOM Sequence

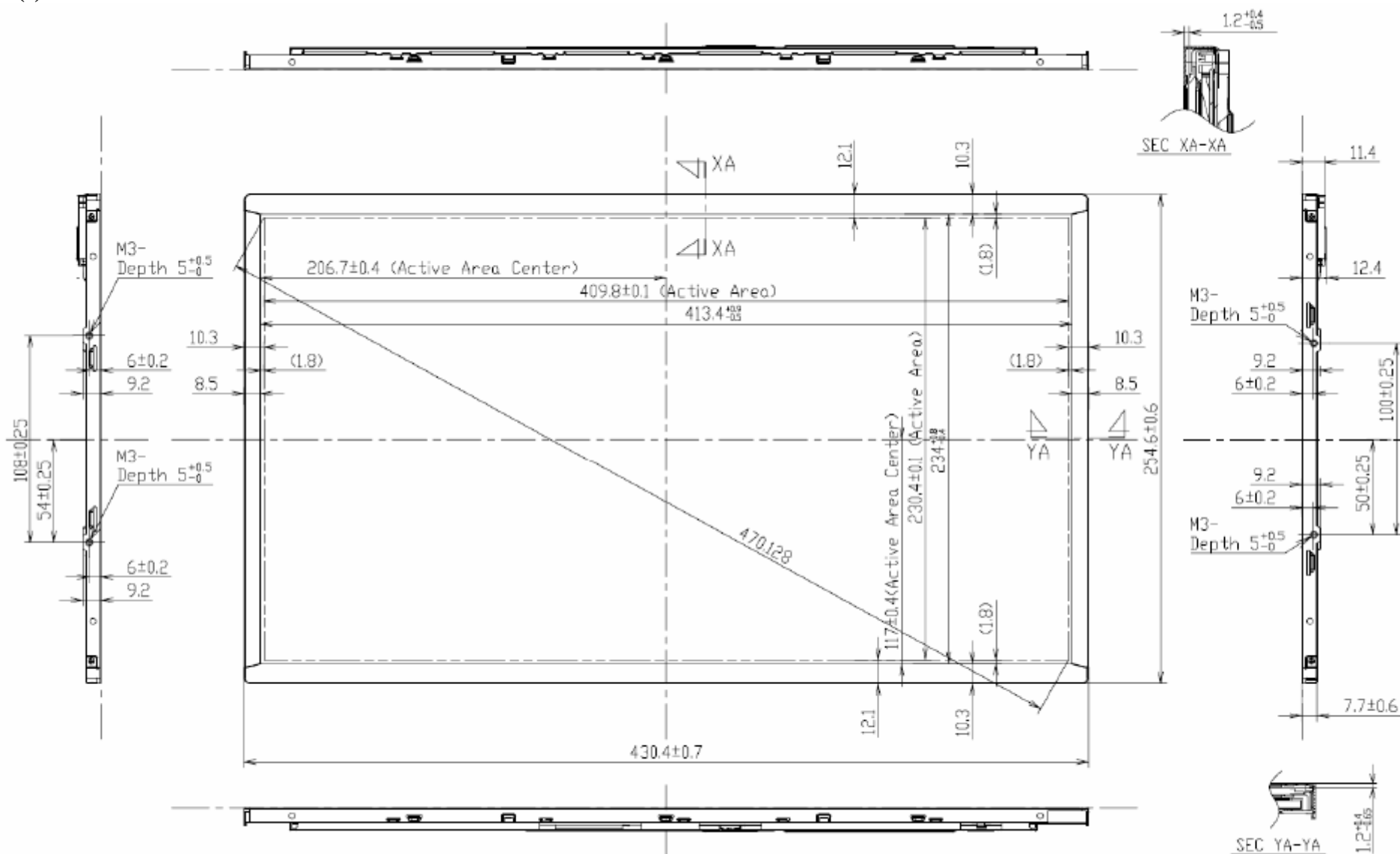


Gate Driver Sequence



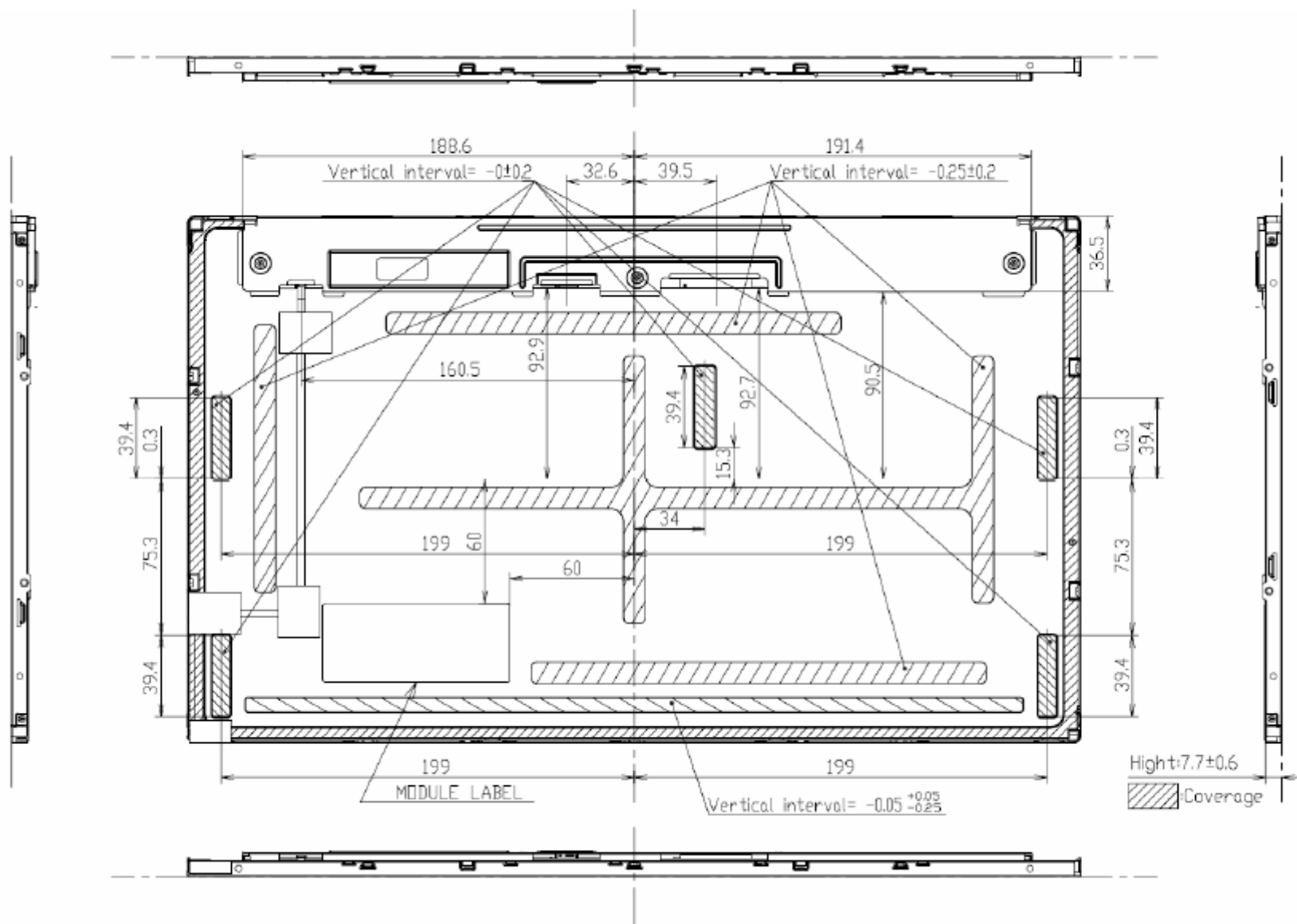
7.DIMENSIONAL OUTLINE

(1) FRONT VIEW



Note 1) Unspecified tolerance to be ± 0.5
 2) User hole torque specification : MAX 0.34N·m (3.5kgf·cm)

(2) BACK VIEW

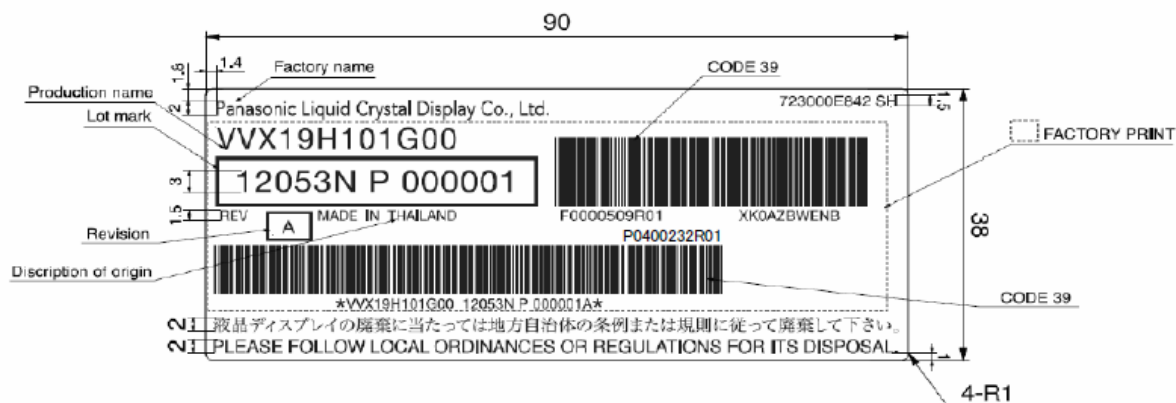


Note 1) Unspecified tolerance to be ± 0.5

8. LABEL FORMAT

8.1 Label

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



REV. is the column for manufacturing convenience. A-Z except I and O may be written on this column.

*** Revision (REV.) control**
Rev. is the column for manufacturing convenience. A-Z except I and O may be written on this column.
(A) --> Mass-Pro (GS) --> 2nd Pre-Pro (ES) --> 1st Pre-Pro (WS) --> ES

*** Lot mark**

6 digits for production number (000001 - 999999)

Special mark 5)

Production management sign 4)

Week of production 3)

Month of production 2)

Year of production 1)

Notes

1) Mark Year

12	2012
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2) Mark Month Mark Month

01	1	07	7
02	2	08	8
03	3	09	9
04	4	10	10
05	5	11	11
06	6	12	12

3) Week mark Day

1	1-7
2	8-14
3	15-21
4	22-28
5	29-31

4) Mark ADDRESS

N	NAKHON RATCHASIMA
---	-------------------

5) Mark RANK

P	CELL-REVISION
---	---------------

9. INSPECTION SPECIFICATION

1. THE ENVIRONMENTAL CONDITION OF INSPECTION

25±5°C, 50±25%RH, 300~500mm distance

Over 600Lux for external appearance inspection(non-operating), upper-lower 15° ; left-right 45° viewing angle

100~200Lux for light on inspection(operating), upper-lower 5° ; left-right 5° viewing angle

2. INSPECTION CONDITION

2.1 Condition of Lot Judgement

(1) Sampling table : ANSI / ASQC Z 1.4

(2) Sampling type : Normal inspection, Single sampling

(3) Inspection Level : I

(4) Acceptable quality level(AQL) : Major defects AQL: 0.4

Minor defects AQL: 1.5

Defects are classified as major defect and minor defect according to the degree of defined herein.

2.2 Classification of Defects

Defects are classified two types, major defect and minor defect according to the defect.

And, the definition of defects is classified as below.

(1) Major defect

Any defect may result in functional failure, or reduce the usability of product for its purpose.

For example, electrical failure, deformation and etc..

(2) Minor defect

A defect that is not to reduce the usability of product for its intended purpose and un-uniformity, dot defect and etc.

The criteria on major and/or minor judgment will be according with the classification of defects.

3. INSPECTION CRITERIA

(1) Definition of dot defect induced from the panel inside.

a) The definition of dot: The size of a defective dot over 1/2 of whole dot is regarded as one defective dot.

b) Bright dot: Dots appear bright and unchanged in size in which module is displaying under black pattern.

bright defect $G > 24.3\%$, $R > 24.3\%$, $B > 24.3\%$

low bright defect $24.3\% \geq G > 4.1\%$, $24.3\% \geq R > 7.8\%$, $24.3\% \geq B > 18.0\%$

c) Dark dot: Dots appear dark and unchanged in size in which module is displaying under pure red, green, blue picture.

d) 2 dot adjacent = 1 pair = 2 dots

pictures:



2 dot adjacent



2 dot adjacent



2 dot adjacent
(Vertical)



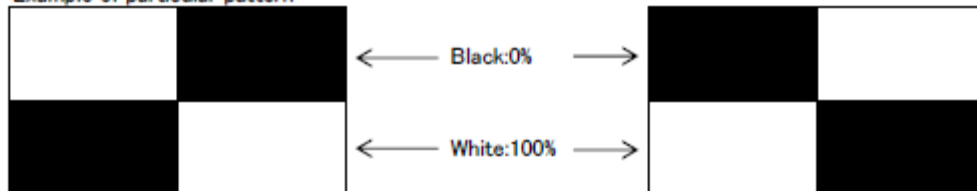
2 dot adjacent
(Slant)

e) 2-dots defect of dark dot applies to B-zone. However, 2-dots defect of dark dot with R and B combination is allowed in C-zone as well.

f) The distance between 2-dots defect of dark dot and other dark dot shall be 20 mm or more.

g) Bright dot with particular(partition) pattern is allowed only in B-zone

Example of particular pattern



(2) Definition of zone

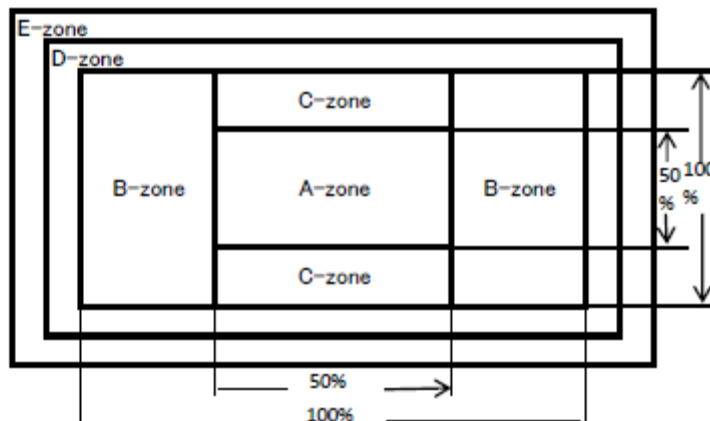
A-zone : Display area (pixel area)

B-zone : Display area (pixel area)

C-zone : Display area (pixel area)

D-zone : Area between E-zone and display area

E-zone : Metallic bezel area



(3) Display Inspection

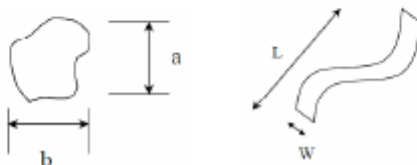
Items			Acceptable count	
			Bright dot	Low Bright dot
Bright dot	Random	Normal	$N \leq 0$	$N \leq 4$
		with partition pattern	$N \leq 1$	
	2 dots adjacent		$N \leq 0$	
	3 dots adjacent or more		$N \leq 0$	
	Density (ϕ 20mm)		$N \leq 0$	
	TOTAL		$N \leq 4$	
Dark dot	Random		$N \leq 7$	
	2 dots adjacent		$N \leq 1$	
	3 dots adjacent or more		$N \leq 0$	
	Density (ϕ 20mm)		$N \leq 3$	
	TOTAL		$N \leq 7$	
Total bright and dark dot			$N \leq 9$	
Display failure (V-line / H-line / Cross line etc.)			Not allowable	

(4) Visual Appearance Specification

Item	Standards
Foreign Black/White/Bright Spot	$0.15 < D \leq 0.5\text{mm}$, $N \leq 4$
Foreign Black/White/Bright Line	$0.05 < W \leq 0.1\text{mm}$, $0.5 < L \leq 5.0\text{mm}$, $N \leq 4$
Polarizer Scratches	$0.05 < W \leq 0.1\text{mm}$, $0.5 < L \leq 10.0\text{mm}$, $N \leq 4$
Dent/Air Bubble	$0.15 < D \leq 0.5\text{mm}$, $N \leq 4$

※ Judge with cell on Backlight.

※ $D=(a+b)/2$



10. PRECAUTION

Please pay attention to the followings when a TFT module with a backlight unit is used, handled and mounted.

10.1 Precaution to handling and mounting

- (1) Applying strong force to a part of the module may cause partial deformation of frame or mold, and cause damage to the display.
- (2) The module should gently and firmly be held by both hands. Never hold by just one hand in order to avoid any internal damage. Never drop or hit the module.
- (3) The module should be installed with mounting holes of a module.
- (4) Uneven force such as twisted stress should not be applied to a module when a module is mounted on the cover case. The cover case must have sufficient strength so that external force can not be transmitted directly to a module.
- (5) It is recommended to leave a space between a module and a holding board of a module so that partial force is not applied to a module.

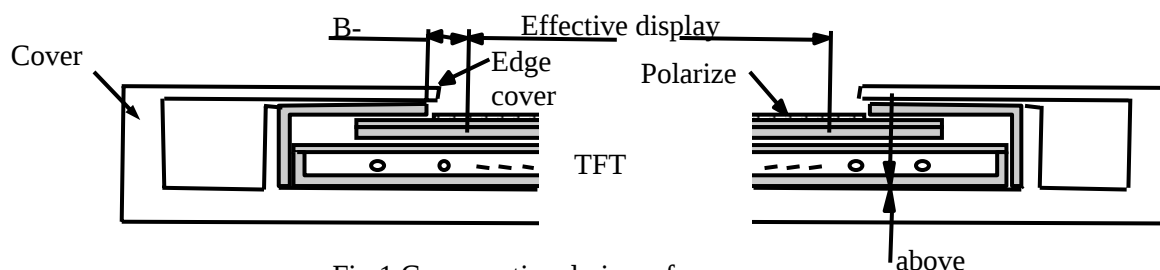


Fig.1 Cross sectional view of a

- (6) The edge of a cover case should be located inside more than 1mm from the edge of a module front frame.
- (7) A transparent protective plate should be added on the display area of a module in order to protect a polarizer and TFT cell. The transparent protective plate should have sufficient strength so that the plate can not touch a module by external force.
- (8) Materials included acetic acid and choline should not be used for a cover case as well as other parts and boards near a module. Acetic acid attacks a polarizer. Choline attacks electric circuits due to electro-chemical reaction.
- (9) The polarizer on a TFT cell should carefully be handled due to its softness, and should not be touched, pushed or rubbed with glass, tweezers or anything harder than HB pencil lead. The surface of a polarizer should not be touched and rubbed with bare hand, greasy clothes or dusty clothes.
- (10) The surface of a polarizer should be gently wiped with absorbent cotton, chamois or other soft materials slightly contained petroleum benzene when the surface becomes dirty. Normal-hexane or Isopropyl alcohol as cleaning chemicals is recommended in order to clean adhesives which fix front/rear polarizers on a TFT cell. Other cleaning chemicals such as acetone, toluen and alcohol should not be used to clean adhesives because they cause chemical damage to a polarizer.
- (11) Saliva or water drops should be immediately wiped off. Otherwise, the portion of a polarizer may be deformed and its color may be faded.
- (12) The module should not be opened or modified. It may cause not to operate properly.
- (13) Metallic bezel of a module should not be handled with bare hand or dirty gloves. Otherwise, color of a metallic frame may become dirty during its storage. It is recommended to use clean soft gloves and clean finger stalls when a module is handled at incoming inspection process and production (assembly) process.
- (14) Lamp(CCFL) cables should not be pulled and held.

10.2 Precaution to operation

- (1) The ambient temperature near the operated module should be satisfied with the absolute maximum ratings. Unless it meets the specifications, sufficient cooling system should be adopted to system.
- (2) The spike noise causes the mis-operation of a module. The level of spike noise should be as follows:

$$-200\text{mV} \leq \text{over- and under- shoot of VDD} \leq +200\text{mV}$$

VDD including over- and under- shoot should be satisfied with the absolute maximum ratings.

- (3) Optical response time, luminance and chromaticity depend on the temperature of a TFT module. Response time and saturation time of LED luminance become longer at lower temperature operation.
- (4) Sudden temperature change may cause dew on and/or in the a module. Dew makes damage to a polarizer and/or electrical contacting portion. Dew causes fading of displayed quality.
- (5) Fixed patterns displayed on a module for a long time may cause after-image. It will be recovered soon.
- (6) A module has high frequency circuits. Sufficient suppression to electromagnetic interference should be done by system manufacturers. Grounding and shielding methods may be effective to minimize the interference.
- (7) Noise may be heard when a backlight is operated. If necessary, sufficient suppression should be done by system manufacturers.
- (8) The module should not be connected or removed while a main system works.
- (9) Inserting or pulling I/F connectors causes any trouble when power supply and signal data are on-state.
I/F connectors should be inserted and pulled after power supply and signal data are turned off.

10.3 Electrostatic discharge control

- (1) Since a module consists of a TFT cell and electronic circuits with CMOS-ICs, which are very weak to electrostatic discharge, persons who are handling a module should be grounded through adequate methods such as a list band.
I/F connector pins should not be touched directly with bare hands.
- (2) Protection film for a polarizer on a module should be slowly peeled off so that the electrostatic charge can be minimized.

10.4 Precaution to strong light exposure

- (1) A module should not be exposed under strong light. Otherwise, characteristics of a polarizer and color filter in a module may be degraded.

10.5 Precaution to storage

When modules for replacement are stored for a long time, following precautions should be taken care of:

- (1) Modules should be stored in a dark place. It is prohibited to apply sunlight or fluorescent light during storage.
Modules should be stored at 0 to 35°C at normal humidity (60%RH or less).
- (2) The surface of polarizers should not come in contact with any other object. It is recommended that modules should be stored in the shipping box of Panasonic Liquid Crystal Display Co.,Ltd.

10.6 Precaution to handling protection film

- (1) The protection film for polarizers should be peeled off slowly and carefully by persons who are electrically grounded with adequate methods such as a list band. Besides, ionized air should be blown over during peeling action. Dusts on a polarizer should be blown off by an ionized nitrogen gun and so on.
- (2) The protection film should be peeling off without rubbing it to the polarizer. Because, if the film is rubbed together with the polarizer, since the film is attached to the polarizer with a small amount of adhesive, the adhesive may remain on a polarizer.
- (3) The module with protection film should be stored on the conditions explained in 10.5 (1). However, in case that the storage time is too long, adhesive may remain on a polarizer even after a protection film is peeled off. Besides, in case that a module is stored at higher temperature and/or higher humidity, adhesive may remain on a polarizer. The remained adhesive may cause non-uniformity of display image.
- (4) The adhesive can be removed easily with Normal-Hexane or Isopropyl alcohol. The remained adhesive or its vestige on the polarizer should be wiped off with absorbent cotton or other soft materials such as chamois slightly contained Normal-Hexane or Isopropyl alcohol.

10.7 Safety

- (1) Since a TFT cell and lamps are made of glass, handling to the broken module should be taken care sufficiently in order not to be injured. Hands touched liquid crystal from a broken cell should be washed sufficiently.

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(2) The module should not be taken apart during operation so that backlight drives by high voltage.

10.8 Environmental protection

Flexible printed circuits and printed circuits board used in a module contain small amount of lead. Please follow local ordinance or regulations for its disposal.

10.9 Use restrictions and limitations

- (1) This product is not authorized for use in life support devices or systems, military applications or other applications which pose a significant risk of personal injury.
- (2) In no event shall Panasonic Liquid Crystal Display Co.,Ltd. be liable for any incidental, indirect or consequential damages in connection with the installation or use of this product, even if informed of the possibility thereof in advance. These limitations apply to all causes of action in the aggregate, including without limitation breach of contract, breach of warranty, negligence, strict liability, misrepresentation and other torts.

10.10 Precaution to setting inverter

- (1) Please use inverter output waveform that satisfies following formulae.

$$0.9 \cdot \sqrt{2} \cdot I_{rms} < |I_p| < 1.1 \cdot \sqrt{2} \cdot I_{rms}$$

$$0.9 \cdot \sqrt{2} \cdot I_{rms} < |I-p| < 1.1 \cdot \sqrt{2} \cdot I_{rms}$$

I_p Peak value of lamp current at positive side

$I-p$ Peak value of lamp current at negative side

Also, please use sine wave with symmetric positive and negative wave that both area and peak of IL and VL waveforms are within 10% of asymmetry rate, and that do not develop spike wave. Otherwise there is a possibility to develop lighting defect.

- (2) After this product is stored for a long time, it might take longer to discharge lamp. It is recommended that auxiliary illuminant (LED, etc.) is set.
- (3) Since multiple lamps are closely-mounted to the backlight, please use inverter that output waveform is synchronized. If different phase inverter is used, it might cause luminance depression or short life span by phase difference.

10.11 Others

Electrical components which may not affect electrical performance are subjective to change without notice because of their availability.